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2003-03

DTV profiles for uncompressed digital video interfaces –

Part 1: General

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DTV PROFILES FOR UNCOMPRESSED DIGITAL VIDEO INTERFACES –

Part 1: General

FOREWORD

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International Standard IEC 62315-1 has been prepared by technical area 4, Digital systems interfaces, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

The text of this standard is based on the following documents:

CDV	Report on voting
100/507/CDV	100/608/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until 2005. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

DTV PROFILES FOR UNCOMPRESSED DIGITAL VIDEO INTERFACES –

Part 1: General

1 Scope

This part of IEC 62315 specifies requirements for digital television (DTV) monitors that use an uncompressed, baseband, digital video interface. These requirements apply to baseband, digital, video interfaces that use the VESA E-EDID™ Standard for the discovery of supported video formats.

This standard also specifies the video formats to be supported by a DTV monitor. The timing requirements for 14 video formats are specified along with requirements for video format discovery. A mechanism allowing a video source to discover the preferred format of a DTV monitor is also described.

A digital video interface is not specified in this part; however, it is envisaged that such interfaces will appear in future parts of IEC 62315.

NOTE 1 It is recommended that devices using the DTV profiles defined in this document, incorporate a digital content protection system on such interfaces in order to ensure interoperability between devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ITU-R BT.601-5: 1995, *Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios*

ITU-R BT.709-5: 2002, *Parameter values for the HDTV standards for production and international programme exchange*

VESA E-EDID™ Standard, *VESA Enhanced Extended Display Identification Data Standard*, Release A, Revision 1, February 9, 2000.

VESA E-DDC™ Standard, *VESA Enhanced Display Data Channel Standard*, Version 1, September 2, 1999.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
aspect ratio
ratio of width to height of a picture or display screen

3.2
aspect ratio, display
aspect ratio of the DTV monitor

3.3
aspect ratio, picture
aspect ratio of the picture, which is made up of the active pixels in the video format

NOTE The pixels are not necessarily square. The video image may be smaller than the active pixel region, with background data filling the rest of the region.

3.4
digital television (DTV)
device that receives, decodes, and presents audio and video material that has been transmitted in a compressed form

NOTE The device may be a single unit or it may be constructed from individual components (e.g. a digital terrestrial set top box and an analogue television).

3.5
digital video interface
cable between a video source and DTV monitor that transfers uncompressed digital video information

3.6
monitor
device capable of displaying video

3.7
monitor, DTV
EDTV, HDTV or SDTV monitor, or any combination of these three

3.8
monitor, EDTV
device capable of displaying 640x480p and either 720x576p or 720x480p in 16:9 or 4:3 aspect ratios

3.9
monitor, HDTV
EDTV monitor, with a 16:9 screen, capable of displaying 1920x1080i or 1280x720p video

3.10
monitor, SDTV
device capable of displaying 720x480i video in 16:9 or 4:3 aspect ratios

3.11
tuner
video source that decodes a digital video transmission and outputs this transmission as video

3.12
tuner, EDTV
tuner capable of converting signals into 640x480p and either 720x576p or 720x480p

3.13
tuner, HDTV
EDTV tuner capable of converting signals into 1920x1080i and 1280x720p

3.14
video source
device that sends video information to a DTV monitor using the digital video interface

4 Symbols and abbreviated terms

ATSC	Advanced Television Systems Committee
DDWG	Digital Display Working Group
DTV	Digital TeleVision
DVI	Digital Visual Interface
E-DDC	Enhanced Display Data Channel
E-EDID	Enhanced Extended Display Identification Data
EDTV	Enhanced Definition Television
EIA	Electronic Industries Alliance
HDTV	High Definition Television
i	interlaced scanning
p	progressive scanning
lsb	least significant bit
LVDS	Low Voltage Differential Signalling
MPEG	Moving Picture Experts Group
MTS	Monitor Timing Specification (a specific VESA standard)
OpenLDI	Open LVDS Display Interface
PSIP	Program and System Information Protocol
SDTV	Standard Definition TeleVision
SMPTE	Society of Motion Picture and Television Engineers
VESA	Video Electronics Standards Association

5 General requirements

Any DTV monitor conforming to this standard shall support the 640x480p format at 60 Hz, as defined in 6.2.1. The DTV monitor shall also support either 720x480p or 720x576p, as defined in 6.2.4 and 6.2.9 respectively, in one of two picture aspect ratios, 4:3 or 16:9. Additionally, any HDTV monitor conforming to this standard shall have a 16:9 display aspect ratio and shall support either 1280x720p or 1920x1080i, as defined in 6.2.2, 6.2.3, 6.2.6, 6.2.7, and 6.2.8. Formats of 720x576i and 720x480i, defined in 6.2.10 and 6.2.5 are optional within this standard.

NOTE 1 This implicitly allows any source device to only support 720x576p, 720x480p, or 640x480p. For the source device to supply high definition content to any HDTV monitor, it should be capable of supporting 1280x720p and 1920x1080i, since an HDTV monitor may only support one of the two formats. In some cases, the source device will need to convert video from its original format (e.g. 720x480i) to a format supported by the DTV Monitor (e.g. 720x480p).

The DTV tuner and DTV monitor requirements specified by this standard are summarized in Table 1. The requirements of 50 Hz applications are different from the requirements of 60 Hz applications, as given in Table 1.

NOTE 2 The product definitions are explained in Clause 3.

Table 1 – Video formats

Product definition	Video format	EDTV monitor	HDTV monitor	EDTV tuner	HDTV tuner
50 Hz applications					
SDTV	720x576i, 50 Hz	o	o	o	o
EDTV	640x480p, 60 Hz	X	X	X*	X*
EDTV	720x576p, 50 Hz	X	X		
HDTV	1280x720p, 50 Hz	o	X*	o	X
HDTV	1920x1080i, 50 Hz	o		o	X
60 Hz applications					
SDTV	720x480i, 60 Hz	o	o	o	o
EDTV	640x480p, 60 Hz	X	X	X*	X*
EDTV	720x480p, 60 Hz	X	X		
HDTV	1280x720p, 60 Hz	o	X*	o	X
HDTV	1920x1080i, 60 Hz	o		o	X

Key
X Required by this standard
X* At least one of the two formats is required, the other is optional
o Optional

6 Waveform timing requirements

Timing parameters shall conform to Table 2 and to the timing diagrams in 6.2. The DTV monitor shall be capable of displaying either 59,94 or 60 Hz (frame rate for progressive scan and field rate for interlaced scan) for those formats listed in Table 1 that it supports. Therefore, the 59,94 Hz and 60 Hz versions of a format shall be considered as the same format with slightly different pixel clocks. DTVs shall accept video when its pixel clock is accurate to within 0.5 % of the clock frequencies specified in Table 2.

Table 2 – Timing parameters for the uncompressed digital video interface

Frequency ±0,5% Hz	Vertical lines			Horizontal pixels		Vertical blanking µs	Horizontal frequency kHz	Pixel frequency MHz	Horizontal blanking µs	Horizontal period µs	Picture aspect ratio	Source of original specification Bibliography reference number
	Active	Total	Interlaced/ progressive	Active	Total							
60	480	525	Progressive	640	800	1429	31,500	25,200	6,35	31,75	4x3	*[17]*
60	1080	1125	Interlaced	1920	2200	667	33,750	74,250	3,77	29,63	16x9	*Normative reference (Clause 2)*
60	720	750	Progressive	1280	1650	667	45,000	74,250	4,98	22,22	16x9	*Normative reference (Clause 2)*
60	480	525	Progressive	720	858	1429	31,500	27,027	5,11	31,75	4x3,16x9	*[5]*
60	480	525	Interlaced	1440*	1716*	1429	15,750	27,027	10,21	63,49	4x3,16x9	*[5]*
50	1080	1125	Interlaced	1920	2640	800	28,125	74,250	9,70	35,56	16x9	*[10]*
50**	1080	1250	Interlaced	1920	2304	2720	31,250	72,000	5,33	32	16x9	*Normative reference (Clause 2)*
50	720	750	Progressive	1280	1980	800	37,500	74,250	9,43	26,67	16x9	*[12]*
50	576	625	Progressive	720	864	1568	31,250	27,000	5,33	32,00	4x3,16x9	*[21]*
50	576	625	Interlaced	1440*	1728*	1568	15,625	27,000	10,67	64,00	4x3,16x9	*[2]*

* The pixels are double-clocked for each line to meet minimum clock speed requirements, thus the active horizontal pixels listed are 1440 rather than 720.

** Some regions are adopting this format instead of 1125 vertical lines in order to improve compatibility with 100 Hz cathode-ray tube televisions.

Timing for the digital video interface on a DTV monitor shall support a base format of 640x480p, 60 Hz.

In countries supporting 50 Hz, the DTV monitor shall support an additional base format of 720x576p, 50 Hz, in at least one of the two picture aspect ratios, 4:3 and 16:9. In countries supporting 60 Hz, the DTV monitor shall support an additional base format of 720x480p, 60 Hz, in at least one of the two picture aspect ratios, 4:3 and 16:9.

An HDTV monitor shall support the timing requirements for either 1280x720p, 1920x1080i, or both, at the frequency appropriate for its country, 50 Hz or 60 Hz.

NOTE The 720x576i, 50 Hz, and 720x480i, 60 Hz, timings are optional.

6.1 Aspect ratio

The 720-line formats (720x576p, 720x576i, 720x480p, 720x480i) are available in two different picture aspect ratios, 4:3 and 16:9. The DTV monitor shall support at least one of these and shall state which picture aspect ratio it supports for a given format (see notes 1 and 2).

The DTV monitor shall list only one picture aspect ratio for a 720-vertical-line format in the E-EDID structure at any given time and the signal shall be processed accordingly (see notes 3 and 4).

NOTE 1 Formats with different picture aspect ratios are considered to be different formats that may be independently supported and discovered.

NOTE 2 The source is able to choose how to supply the picture aspect ratio that a DTV monitor supports. For example, with the 16x9 data format and a 4x3 DTV monitor, the source may:

a) use pan and scan information to crop the data to fewer horizontal pixels and then resample up to the required pixels for output to the DTV monitor, or

b) vertically resample and create blank panels above and below the picture to send this “letterbox” with the required lines for output.

Other picture scaling methods are possible in either the video source or DTV monitor. For example, picture aspect scaling (picture expand, shrink, etc.) can be accomplished in the video source, such as adding black lines in the active video portion of the signal for non-standard picture aspect ratios.

NOTE 3 It is possible for a DTV monitor to support both aspect ratios of the 720x480 formats through a user-selectable option on the DTV monitor. In this case, the E-EDID timing descriptor may be changed to reflect the user-requested picture aspect ratio. Video sources should have a method for tracking changes to user-selected aspect ratios.

NOTE 4 As shown in the timing diagrams (see 6.2), there is no difference in the timing parameters for formats that have different picture aspect ratios but are otherwise the same format. For a DTV monitor to simultaneously support both formats, the DTV monitor requires an indication from the source that describes the aspect ratio in which the video should be displayed These involve sending picture aspect ratio information from a video source to the DTV monitor. It is envisaged that future parts of this standard will provide standardized methods to accomplish this task.

6.2 Timing diagrams

6.2.1 640x480p, 59,94/60 Hz

The timing parameters for 640x480p, 59,94/60 Hz, shall be as illustrated in Figure 1.

NOTE This timing is based on *VESA Monitor Timings Specification,* version 1.0 revision 0.8 [16]*. The only difference is that the VESA version defines blanking to not include the border, while this standard includes the border within the blanking interval.

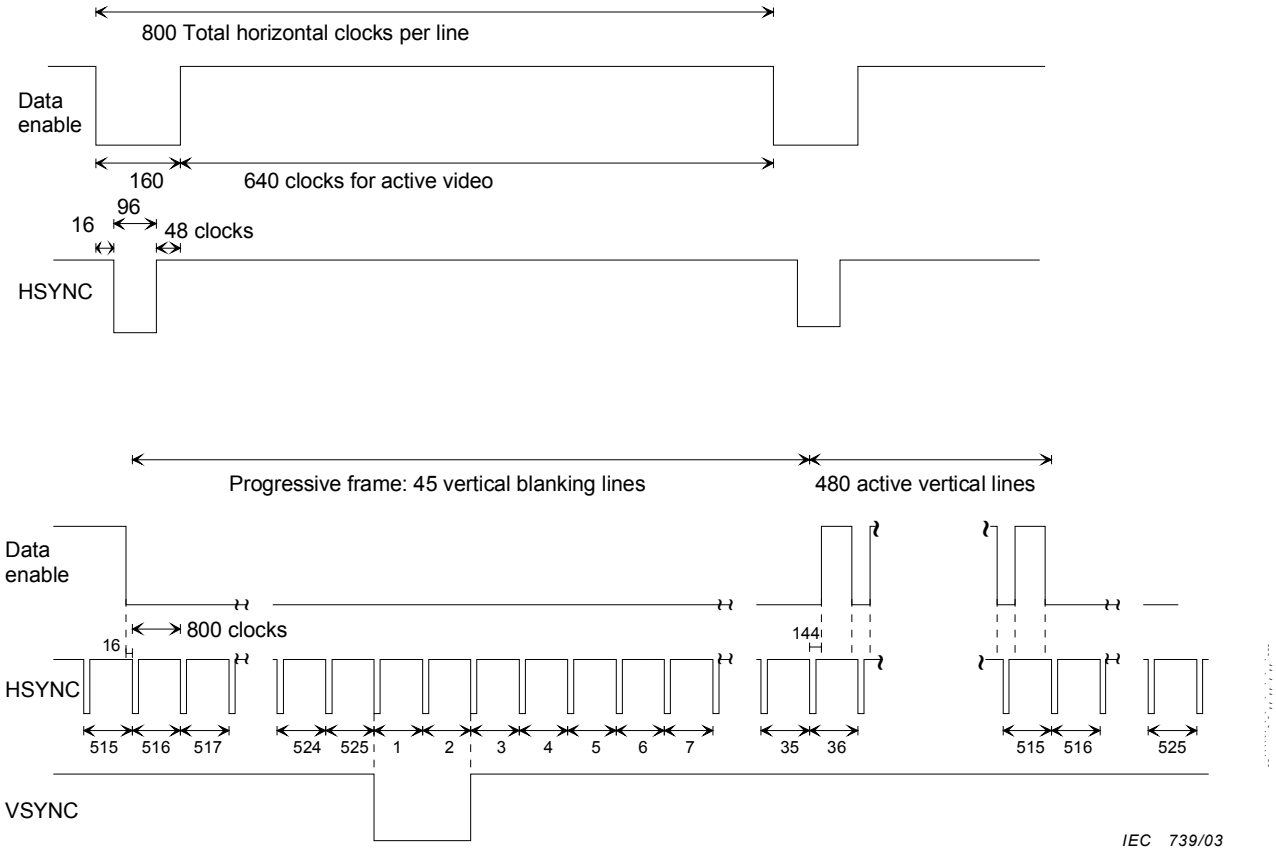


Figure 1 – Timing parameters for 640x480p, 59,94/60 Hz

* Figures in square brackets refer to the bibliography.

6.2.2 1280x720p, 59,94/60 Hz

The timing parameters for 1280x720p, 59,59/60 Hz, shall be as illustrated in Figure 2. This format uses a 16:9 aspect ratio.

NOTE This timing is based on EIA-770.3-C [6], but there are two differences. First, EIA-770.3-C uses tri-level sync, while this standard uses bi-level. Bi-level sync timing is accomplished using the second half of the EIA-770.3-C tri-level sync, defining the actual sync time to be the rising edge of that pulse. Second, EIA-770.3-C uses a composite sync while this standard uses separate sync signals, thus eliminating the need for serrations during vertical sync.

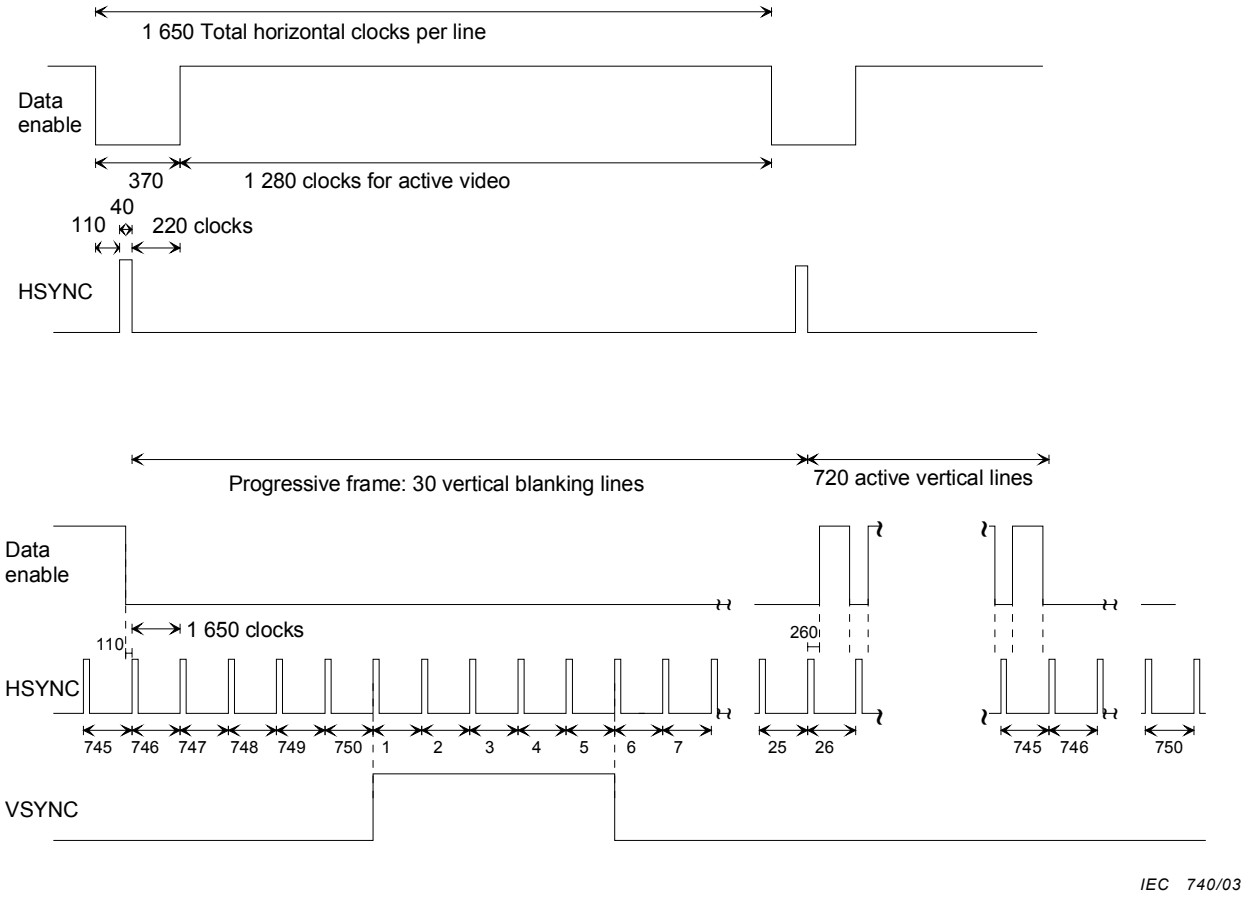


Figure 2 – Timing parameters for 1280x720p, 59,94/60 Hz

6.2.3 1920x1080i, 59,94/60 Hz

The timing parameters for 1920x1080i, 59,59/60 Hz, shall be as illustrated in Figure 3. This format uses a 16:9 aspect ratio.

NOTE This timing is based on EIA-770.3-C [6], but there are two differences. First, EIA-770.3-C uses tri-level sync, while this standard uses bi-level. Bi-level sync timing is accomplished using the second half of the EIA-770.3-C tri-level sync, defining the actual sync time to be the rising edge of that pulse. Second, EIA-770.3-C uses a composite sync while this standard uses separate sync signals, thus eliminating the need for serrations during vertical sync.

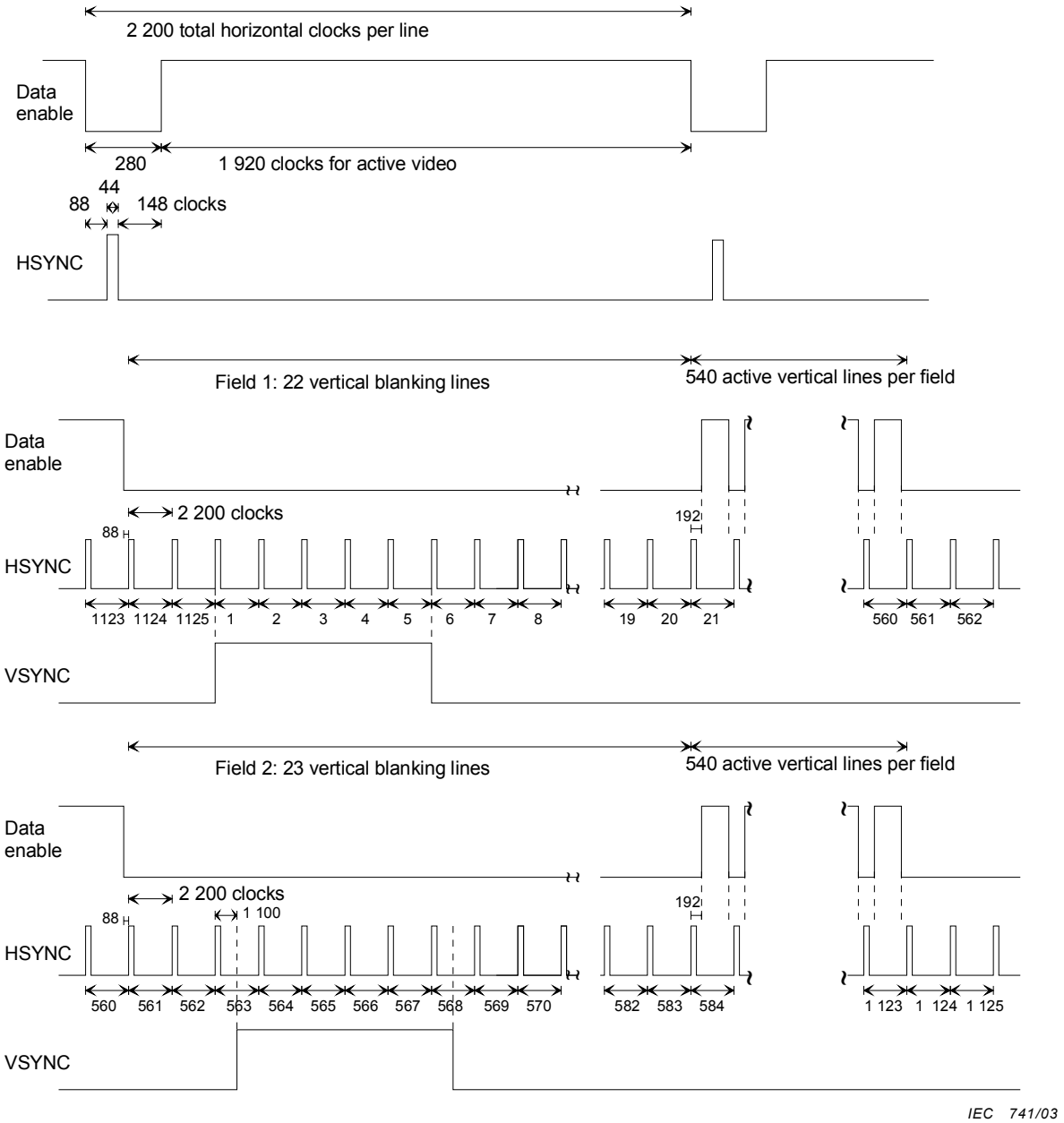


Figure 3 – Timing parameters for 1920x1080i, 59,94/60 Hz

6.2.4 720x480p, 59,94/60 Hz

The timing parameters for 720x480p, 59,59/60 Hz, shall be as illustrated in Figure 4. This format can use either 4:3 or 16:9 picture aspect ratio. The DTV tells the video source, through the EDID structure, which format it supports. The video source then formats the picture and scales the horizontal resolution for proper display.

NOTE This timing is based on EIA-770.2-C [5], with one difference. EIA-770.2-C has a composite sync while this standard uses separate sync signals, thus eliminating the need for serrations during vertical sync.

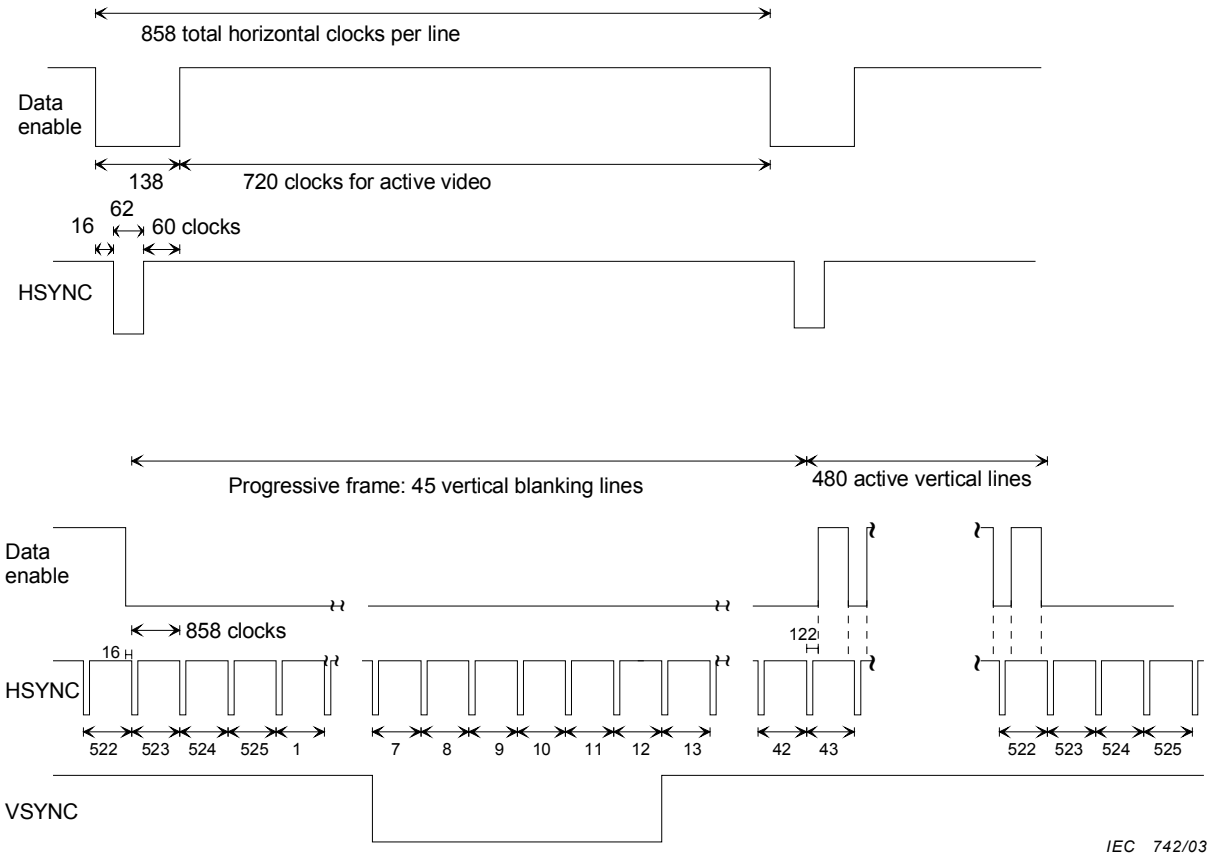


Figure 4 – Timing parameters for 720x480p, 59,94/60 Hz

6.2.5 720x480i, 59,94/60 Hz

The timing parameters for 720x480i, 59,59/60 Hz, shall be as illustrated in Figure 5. This format can use either 4:3 or 16:9 picture aspect ratio. The DTV tells the video source, through the EDID structure, which format it supports. The video source then formats the picture and scales the horizontal resolution for proper display.

NOTE This timing is based on EIA-770.2-C [5], with a few differences. Whereas EIA-770.2-C has a composite sync, this format uses separate sync signals, thus eliminating the need for serrations during vertical sync. Whereas EIA-770.2-C uses conventional clocking, this format assumes the pixels are double clocked to meet minimum clock speed requirements of the interface.

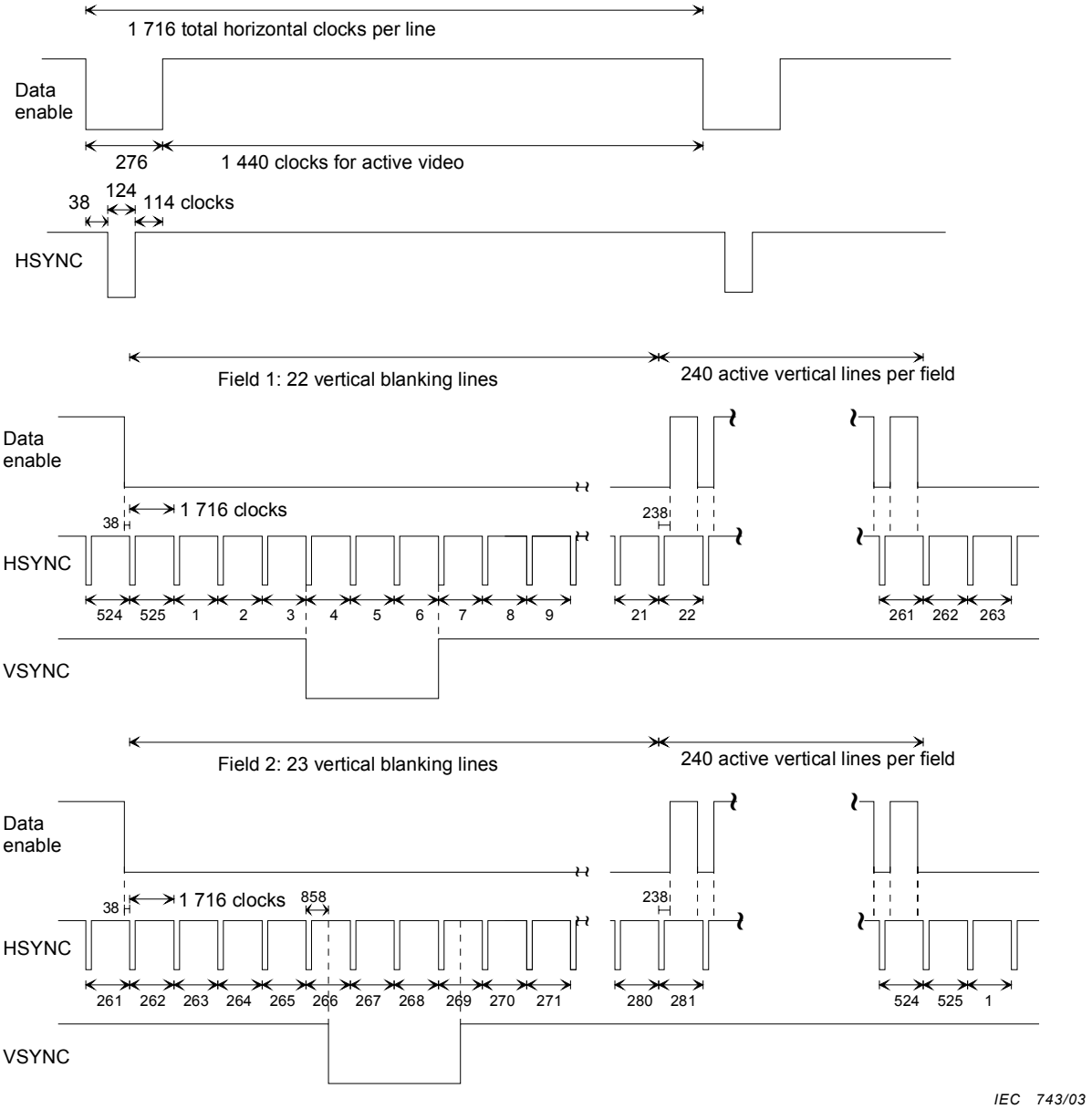


Figure 5 – Timing parameters for 720x480i, 59,94/60 Hz

6.2.6 1280x720p, 50 Hz

The timing parameters for 1280x720p, 50 Hz, shall be as illustrated in Figure 6. This format uses a 16:9 aspect ratio.

NOTE This timing is based on SMPTE 296M [12], but there are two differences. First, SMPTE 296M uses tri-level sync, while this standard uses bi-level. Bi-level sync timing is accomplished using the second half of the SMPTE 296M tri-level sync, defining the actual sync time to be the rising edge of that pulse. Second, SMPTE 296M uses a composite sync while this standard uses separate sync signals, thus eliminating the need for serrations during vertical sync.

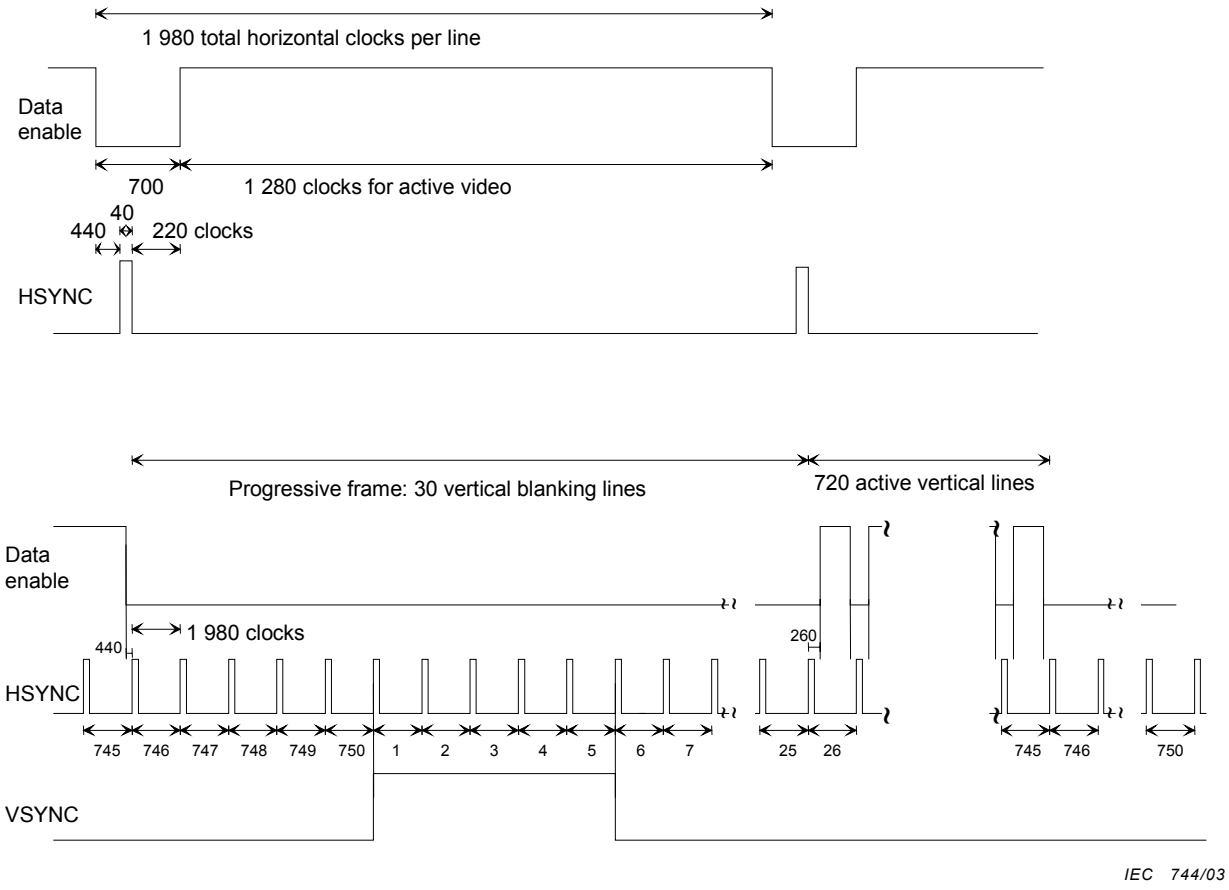


Figure 6 – Timing parameters for 1280x720p, 50 Hz

6.2.7 1920x1080i (1125 total lines), 50 Hz

The timing parameters for 1920x1080i, 1125 total lines, 50 Hz, shall be as illustrated in Figure 7. This format uses a 16:9 aspect ratio.

NOTE This timing is based on SMPTE 274M [10], but there are two differences. First, SMPTE 274M uses tri-level sync, while this standard uses bi-level. Bi-level sync timing is accomplished using the second half of the SMPTE 274M tri-level sync, defining the actual sync time to be the rising edge of that pulse. Second, SMPTE 274M uses a composite sync while this standard uses separate sync signals, thus eliminating the need for serrations during vertical sync.

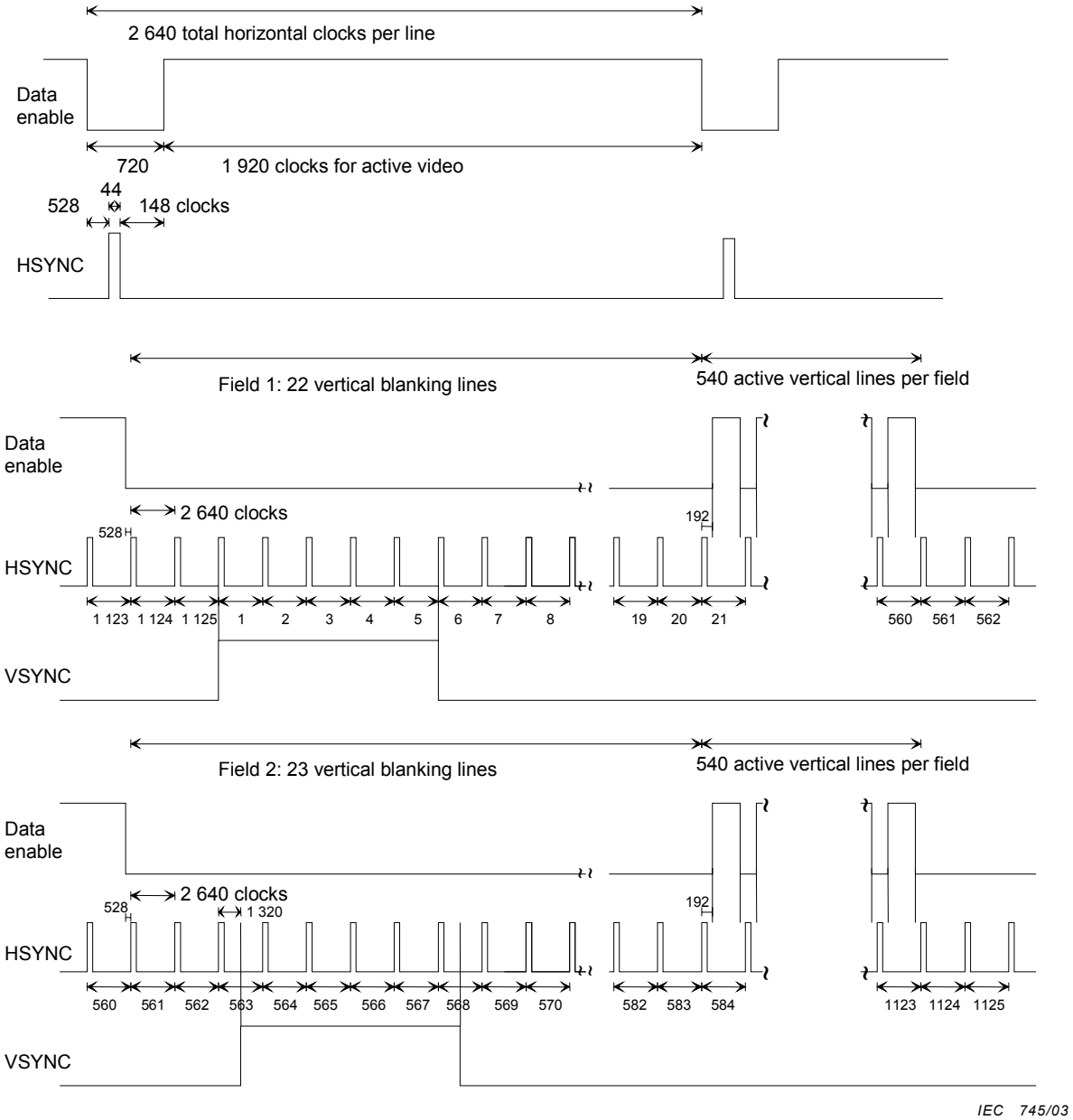
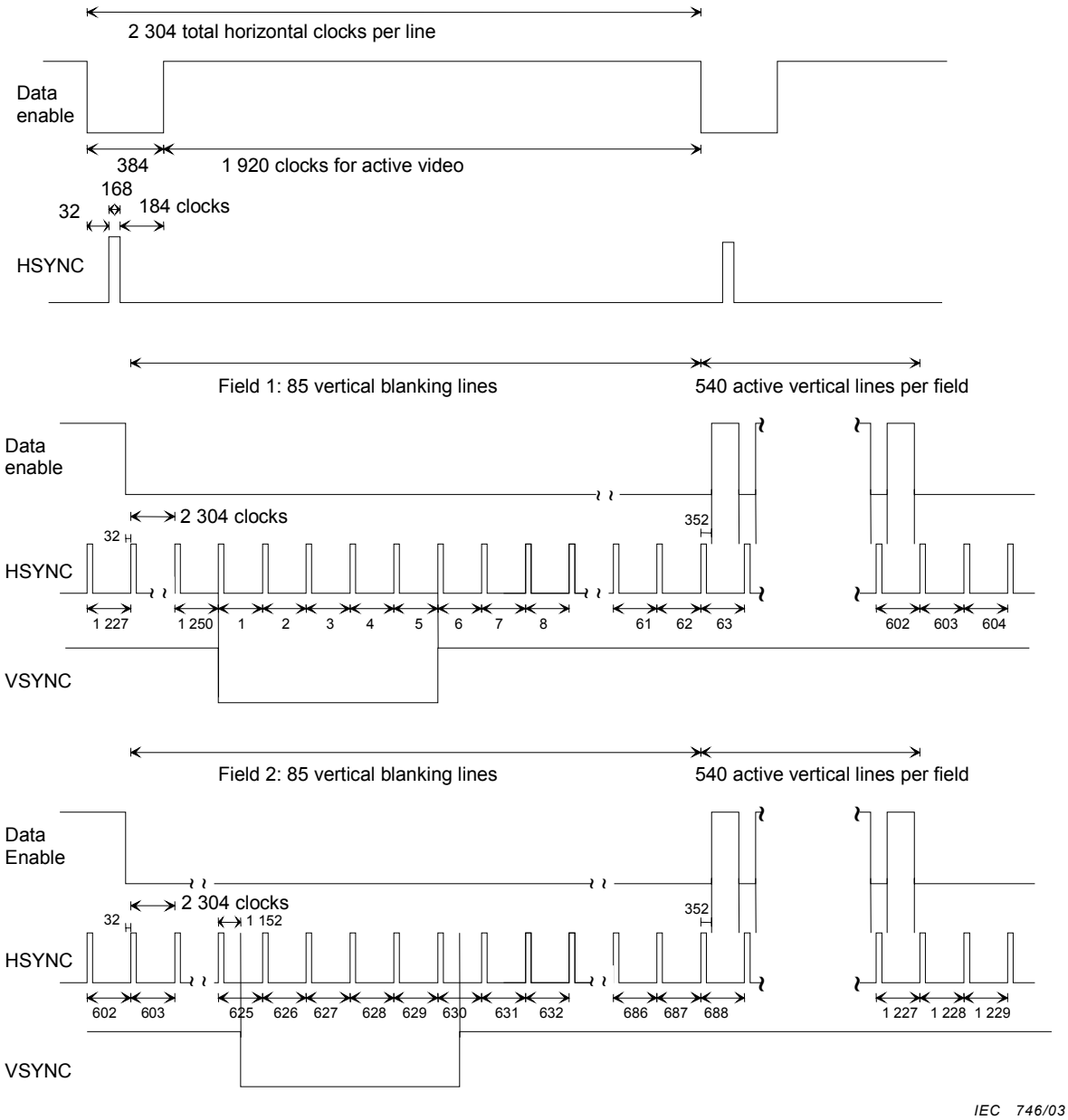


Figure 7 – Timing parameters for 1920x1080i (1125 total lines), 50 Hz

6.2.8 1920x1080i (1250 total lines), 50 Hz

The timing parameters for 1920x1080i, 1250 total lines, 50 Hz, shall be as illustrated in Figure 8. This format uses a 16:9 aspect ratio.

NOTE This format is based on ITU-R BT.709-5, but there are two differences. First, there are 1080 active lines instead of 1152, secondly, ITU-R BT.709-5 use tri-level sync, while this standard uses bi-level sync.



First field = 624,5 lines ; second field = 625,5 lines

Figure 8 – Timing parameters for 1920x1080i (1250 total lines), 50 Hz

6.2.9 720x576p, 50 Hz

The timing parameters for 720x576p, 50 Hz, shall be as illustrated in Figure 9. This format can use either 4:3 or 16:9 picture aspect ratio. The DTV tells the video source, through the EDID structure, which format it supports. The video source then formats the picture and scales the horizontal resolution for proper display.

NOTE This timing is based on ITU-R BT.1358 [4]. The DTV tells the video source, through the EDID structure, which formats it supports. The video source then formats the picture and scales the horizontal resolution for proper display.

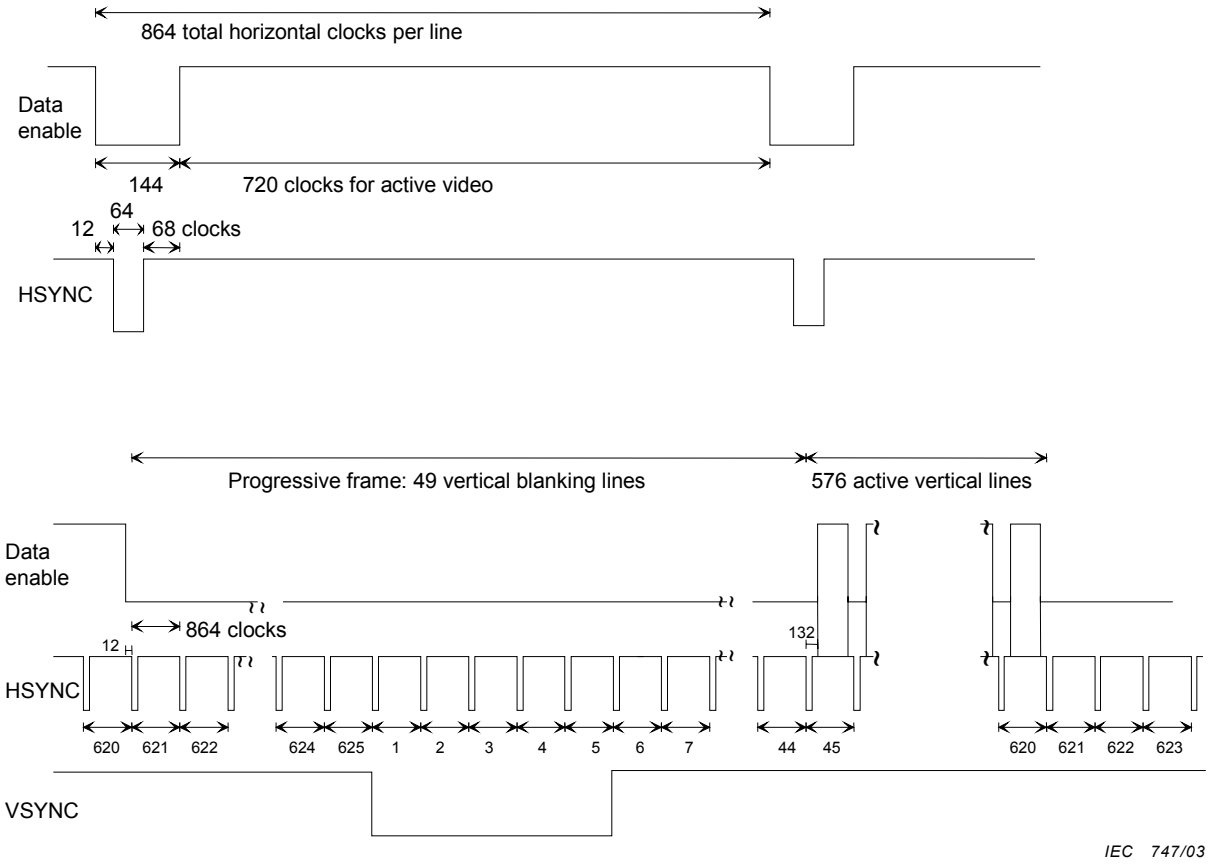


Figure 9 – Timing parameters for 720x576p, 50 Hz

6.2.10 720x576i, 50 Hz

The timing parameters for 720x576i, 50 Hz, shall be as illustrated in Figure 10. This format can use either 4:3 or 16:9 picture aspect ratio. The DTV tells the video source, through the EDID structure, which format it supports. The video source then formats the picture and scales the horizontal resolution for proper display.

NOTE This timing is based on ITU-R BT.656–4 [2] except for horizontal and vertical synchronization pulses duration which are based on ITU-R BT.711–1 [3] and ITU-R BT.470–6 [1]. This format assumes the pixels are double clocked to meet minimum clock speed requirements for the interface. Thus, the clock is 27 MHz. The DTV monitor tells the video source, through the EDID structure, which formats it supports. The video source then formats the picture and scales the horizontal resolution for proper display.

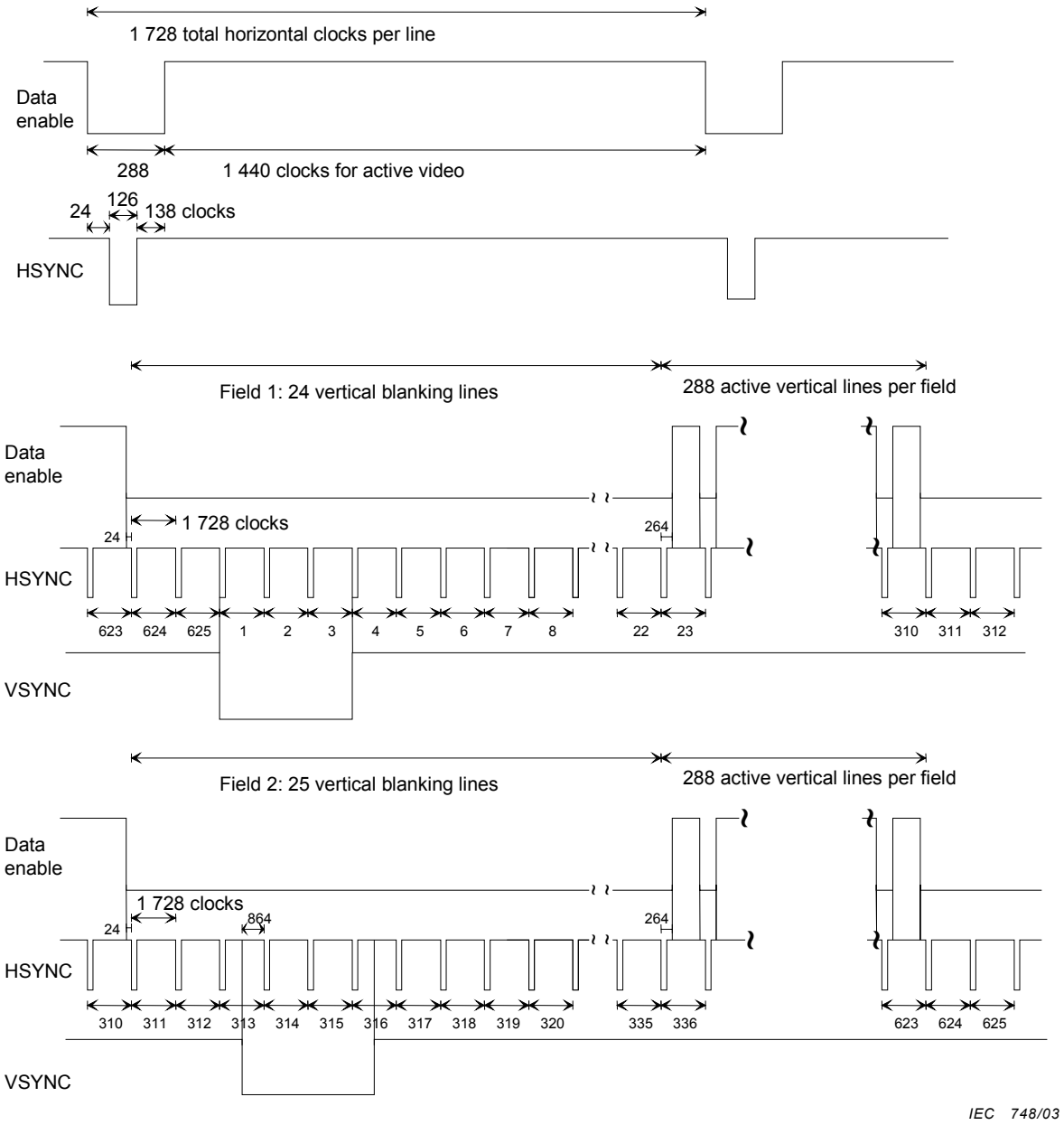


Figure 10 – Timing parameters for 720x576i, 50 Hz

6.3 Format requirements summary

The required support for the formats defined in this standard is summarized in Table 3.

Table 3 – Summary of video format requirements

Format	Field rate	Picture aspect ratio (H:V)	Pixel aspect ratio (H:V)	Requirement on DTV monitor
50 Hz countries				
640x480p	59,94 Hz, 60 Hz	4:3	1:1	Required
720x576p	50 Hz	4:3	8:9	At least one of these two is required
720x576p	50 Hz	16:9	32:27	
1280x720p	50 Hz	16:9	1:1	Optional, but at least one format shall be supported by an HDTV monitor.
1920x1080i	50 Hz	16:9	1:1	
720x576i	50 Hz	4:3	8:9	Optional
720x576i	50 Hz	16:9	32:27	Optional
60 Hz countries				
640x480p	59,94 Hz, 60 Hz	4:3	1:1	Required
720x480p	59,94 Hz, 60 Hz	4:3	8:9	At least one of these two is required
720x480p	59,94 Hz, 60 Hz	16:9	32:27	
1280x720p	59,94 Hz, 60 Hz	16:9	1:1	Optional, but at least one format shall be supported by an HDTV monitor.
1920x1080i	59,94 Hz, 60 Hz	16:9	1:1	
720x480i	59,94 Hz, 60 Hz	4:3	8:9	Optional
720x480i	59,94 Hz, 60 Hz	16:9	32:27	Optional

7 Colorimetry

The colorimetry of this interface shall be RGB (red, green, and blue), with encoding parameters based on the format.

7.1 640x480p, 720x480p, 720x480i, 720x576p, and 720x576i

ITU-R BT.601-5, subclause 3.5 shall be used for any colour space conversion needed in the course of processing. The encoding parameter values shall be as defined in Table 3 of ITU-R BT.601-5 and as summarized in (a) through (d):

a) The scale of the signal shall be 0 to 255 (8-bit coding).

b) The R, G, and B signals shall have 220 quantization levels

c) The black level shall correspond to level 16.

d) The peak white level shall correspond to level 235.

In addition, the 640x480p format is an exception to these rules and shall use all 256 quantization levels.

NOTE 1 The colour space used by the 480-line and 576-line formats is most commonly based on ITU-R BT.470–6 [1]. The service provider (e.g., cable, satellite, terrestrial, etc.) is expected to signal to the video source which colour space is being transmitted and associate it with the video content.

NOTE 2 If a signal includes black levels below 16, these should be ignored and treated as 16. If a signal includes white levels above 235, these should be ignored and treated as 235.

NOTE 3 It is envisaged that future Parts of this standard will provide signalling for alternate colour space conversions.

7.2 1920x1080i and 1280x720p

Any colour space conversion needed in the course of processing shall be in accordance with ITU-R BT.709-5 Part 1, Clause 4.

The digital representation shall be as defined in BT.709-4 Part 1, Section 6.10 and is summarized below:

a) the coding shall be 8-bit coding;

b) the black level shall correspond to level 16;

c) the nominal peak shall be 235.

BT.709-4 requires 480i format video signals to use 0.0 IRE black level set-up.

NOTE A digitized analogue signal may inadvertently use the 7.5 IRE black level set-up. In this case, the video source should change the black level to 0.0 IRE.

8 E-EDID structure

The data structure used to describe timing formats shall conform to VESA E-EDID Data Structure Version 1, Revision 3 as described in VESA Enhanced Extended Display Identification Data Standard, Release A, Revision 1, February 9, 2000, (E-EDID). The DTV monitor shall support VESA Enhanced Display Data Channel Standard, Version 1, September 2, 1999, (E-DDC) as the method of transporting E-EDID information. In 59,94 Hz or 60 Hz applications, a DTV monitor shall support both the 60 Hz and 59,94 Hz version of any format it supports. The 60 Hz version shall be described in the EDID structure for HDTV formats, the 59,94 Hz version shall be described for all 480-line formats.

The preferred timing format shall be described in the first 18-byte “detailed timing descriptor” and shall include the Display Aspect Ratio. Two of the four 18-byte descriptors contained in E-EDID Block 0 are reserved for a monitor Range Limits Descriptor and a monitor Name Descriptor. Consequently, the E-EDID standard provides a method for including only two detailed timing descriptors, while twelve new DTV formats are defined in this standard.

NOTE 1 The first timing descriptor indicates a DTV monitor's most preferred format. When more that one format can be transmitted from the source, the preferred format should be used.

NOTE 2 The E-EDID standard can accommodate additional timing formats.

If a DTV monitor supports more than two video formats from this standard, the structure specified in Annex C shall be used to include any additional 18-byte detailed timing descriptors necessary to describe all the formats. Therefore, the DTV monitor shall enumerate all of the DTV formats that it supports in E-EDID block 0 and in the newly defined extension block. The timing extension examples in Annex D specify formats, using data blocks provided in the E-EDID standard. Consistent with other applications, it is not necessary to enumerate 640x480p, since this format is required to be supported in all cases.

The E-EDID 18-byte detailed timing descriptor allows the designation of an interlaced format; however, there is no method to specify separate vertical blanking intervals or sync offsets for Field 1 and Field 2. Therefore, the following rules apply for interlaced formats:

a) the Field 1 Vertical Blanking Interval shall equal the Vertical Blanking Lines in the Detailed Timing Descriptor;

b) the Field 2 Vertical Blanking Interval shall equal the Vertical Blanking Lines in the Detailed Timing Descriptor + 1;

c) the Field 1 Vertical Sync Offset shall equal the Vertical Sync Offset in the Detailed Timing Descriptor;

d) the Field 2 Vertical Sync Offset shall equal the Vertical Sync Offset in the Detailed Timing Descriptor + 1/2.

As different EDID structures are required for formats with different picture aspect ratios, the vertical and horizontal image size parameters shall contain numbers that describe the aspect ratio of the displayed video.

NOTE 3 Actual image dimensions are preferred, but not required.

There shall be two cases, either 4:3 or 16:9, which are calculated by the video source by dividing the width by the height.

NOTE 4 Unless signalling of the display aspect ratio is provided and supported across the digital interface, a DTV monitor must display a format, such as 720x576p or 720x480p, in one set aspect ratio (either 4:3 or 16:9). Other parts of this multi-part standard will specify methods to send picture aspect ratio information from the video source to the DTV monitor. Therefore, it is possible that video sources will encounter descriptors for both aspect ratios within a single DTV monitor. To allow for this possibility, it is recommended that video sources consider the first occurrence of the format in the E-EDID to be the displayed format, in the absence of aspect ratio information being carried from the video source to the DTV monitor. It is also recommended that DTV monitors place the descriptor for their preferred aspect ratio before any descriptor with other picture aspect ratios for the same format within the E-EDID structure.

Annex A
(informative)

Application to DVI

A.1 General

This annex describes Digital Visual Interface (DVI), one of the digital video interfaces capable of supporting this standard.

A.2 DVI synchronization

The synchronizing signals are carried in the same manner as other control words, using 7-transition words (as opposed to the 5-transition words used for video data). The Hsync and Vsync are sent as C1 and C0 with the blue channel, and are sent when the data enable signal (DE) is low. Table A.1 shows the 10-bit code words used for each of the four possible states of the Hsync-Vsync signal pair.

Table A.1 – Synchronizing signal data for DVI

State	C1	C0	10-bit Code word
Both low	0	0	0010101011
Vsync high	0	1	1101010100
Hsync high	1	0	0010101010
Both High	1	1	1101010101

A.3 Connector and cable

The connector is DVI-Digital, Single Link [10].

The cable supplied with the product is capable of reliably carrying the signal with the maximum pixel clock frequency compatible with the product.

A.4 Digital Content Protection

High-bandwidth Digital Content Protection (HDCP) (see *High-bandwidth Digital Content Protection System* [20]) is available to authenticate display devices and encrypt content transmitted across the DVI interface. This ensures full interoperability of devices.

Annex B
(informative)

Application to OpenLDI

B.1 General

This annex describes OpenLDI, one of the digital video interfaces capable of supporting this standard.

B.2 OpenLDI data and control signals

OpenLDI has two options for display synchronization:

DC balance mode;

Non DC balance mode.

In DC balance mode, synchronization is accomplished by transmitting control signals during the display blanking intervals as shown in Figure B.1.

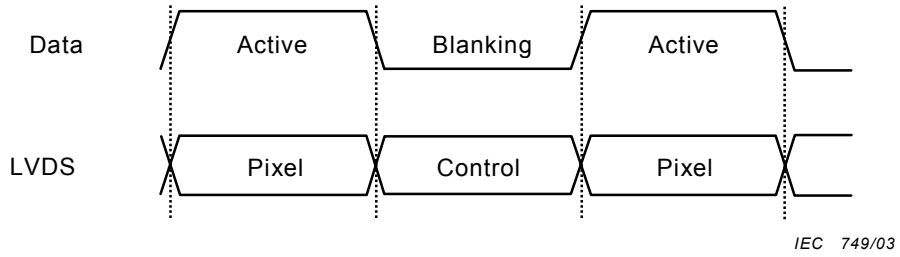


Figure B.1 – OpenLDI synchronization

In the single or dual LVDS bus mode (24 or 48 bit total), the control signals are transmitted over 7 transition words on specific output signals during the blanking period as shown in Table B.1.

Table B.1 – OpenLDI control signals

Control signal	Signal level	Output signal	Data pattern
DE	High	CLK1 and CLK2	1111000 or 1110000
	Low		1111100 or 1100000
HSYNC	High	A0	1100000 or 1111100
	Low		1110000 or 1111000
VSYNC	High	A1	1100000 or 1111100
	Low		1110000 or 1111000

B.3 Non-DC-balanced mode

Control signals are transmitted as part of the LVDS serialized data stream. The control signals are then de-serialized and regenerated at the receiver outputs to the EDTV/HDTV monitor.

B.4 OpenLDI cabling information

An OpenLDI cable assembly consists of a cable meeting the requirements of this clause with an OpenLDI plug on each end or an OpenLDI plug on one end and the other end permanently affixed to the display device.

Cable length
The maximum cable length is 10 m.

Number of signal conductors
The OpenLDI cable comprises 11 twisted pairs and 10 individual conductors.

Wire gauge
Each conductor in an OpenLDI cable is no less than 28 AWG.

Conductor resistance
The resistance of a single conductor of an OpenLDI cable does not exceed 4 Ω when the conductor is of the maximum length specified in this standard.

Insulation
Each conductor in the cable is separately insulated. The minimum insulation resistance is 1 GΩ.

Shield requirement
The OpenLDI cable is encompassed by a single shield, surrounding all conductors in the cable. The shield provides a minimum of 90 % coverage.

For shielded twisted pair cable, each twisted pair is shielded individually. Each shield provides a minimum of 90 % coverage.

Single twisted pair transmission skew
The differential time of transmission (single pair transmission skew) of a pulse through a single differential pair in an OpenLDI cable does not exceed 300 ps.

Multiple twisted pair transmission skew
The differential time of transmission (pair to pair transmission skew) of a pulse through any two differential pairs in an OpenLDI cable does not exceed 1 bit time.

USB cable requirements
The conductors used for transmission of USB signals on the OpenLDI cable meet the requirements stated in the Universal Serial Bus Specification, Version 1.0, January 15, 1996 [21].

DDC cable requirements
The conductors used for transmission of DDC signals on the OpenLDI cable meet the requirements stated in the VESA Display Data Channel Command Interface (DDC/CI) Standard, Version 1, August 14, 1998 [17].

Annex C
(normative)

E-EDID timing extension

The following E-EDID extension follows the format described in 2.2.1.3 of VESA Enhanced Extended Display Identification Data Standard, Release A, Revision 1. The parts of the extension applicable to this standard are specified in Table C.1. The EDID extension tag for this extension shall be 02h.

Table C.1 – E-EDID extension block that contains extra detailed timing descriptors

Byte #	Value	Description	Format
0	02 h	Tag (02 h)	
1	01 h	Revision number	
2		Byte number offset *d* where Detailed Timing data begins	*d* = offset for the byte following the last 8-byte timing description. If no 8-byte descriptions are provided, then *d*=4. If no detailed timing descriptions are provided then *d*=0.
3	00 h	Reserved (places descriptors on even byte boundary)	Set to 00 h
4		Start of short descriptions	
d-1		End of short descriptions	
d		Start of 18-byte detailed timing descriptions	See **3.10.2** of VESA E-EDID Standard
d+(18 x *n*)-1		End of 18-byte detailed timing descriptions where *n* is the number of descriptors included	
d+(18 x *n*)	00 h	Beginning of padding	
126	00 h	End of padding	
127		Checksum	xxh = This byte shall be programmed such that a one-byte checksum (add all bytes together) of the entire 128 byte block equals “00 h”.

Annex D
(informative)

Example E-EDID 18-byte detailed timing descriptors

Tables D.1 to D.12 illustrate recommended detailed timing descriptor values for the formats described in this standard. While the image size (bytes 42 h and 43 h) may vary, the remaining values should be used.

Table D.1 – Example detailed timing descriptor for 1280x720p (50 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (LSB stored first)	01	Pixel clock = 74,25 MHz
37		1D	
38	Horizontal active pixels (lower 8 bits)	00	Horizontal active pixels = 1280 = 500 h
39	Horizontal blanking pixels (lower 8 bits)	BC	Horizontal blanking pixels = 700 = 2BC h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	52	
3B	Vertical active lines, lower 8 bits	D0	Vertical active lines = 720 = 2D0 h
3C	Vertical blanking lines, lower 8 bits	1E	Vertical blanking lines = 30 = 1E h
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	B8	Offset = 440 pixels = 1B8 h
3F	Horizontal sync pulse width (pixels, lower 8 bits)	28	Width = 40 pixels = 28 h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55	Vertical sync. offset = 5 lines Vertical sync width = 5 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	80	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	00	0
46	Vertical border (pixels)	00	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1–4 = sync description; bit 0 = don't care)	1E	Flag = non-interlaced; non-stereo; digital separate; positive V sync; positive H sync

Table D.2 – Example detailed timing descriptor for 1920x1080i (50 Hz, 16:9, 1125 lines)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	01	Pixel clock = 74,25 MHz
37		1D	
38	Horizontal active pixels (lower 8 bits)	80	Horizontal active pixels = 1920 = 780 h
39	Horizontal blanking pixels (lower 8 bits)	D0	Horizontal blanking pixels=720 = 2D0 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	72	
3B	Vertical active lines, lower 8 bits	1C	Vertical active lines = 540 = 21C h
3C	Vertical blanking lines, lower 8 bits	16	Vertical blanking lines = 22 = 16 h
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	10	Offset = 528 pixels = 210 h
3F	Horizontal sync pulse width (pixels, lower 8 bits)	2C	Width = 44 pixels = 2C h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	25	Vertical sync. offset = 2 lines Vertical sync width = 5 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	80	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	00	0
46	Vertical border (pixels)	00	0
47	Flags (bit 7 = interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	9E	Flag = interlaced; non-stereo; digital separate; positive Vsync; positive Hsync

[a] For interlaced display: field 1 vertical blanking = Vertical blanking lines. Field 2 vertical blanking = Vertical blanking lines + 1 line.

[b] For interlaced display: field 1 vertical offset = Vertical sync offset. Field 2 vertical offset = Vertical sync offset + 0,5 lines.

[c] Image size is display dependent. Ratio of horizontal image size to vertical image size shall be 16:9 or 4:3.

Table D.3 – Example detailed timing descriptor for 720x576p (50 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	D0	Horizontal active pixels = 720 = 2D0 h
39	Horizontal blanking pixels (lower 8 bits)	90	Horizontal blanking pixels = 144 = 90 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3B	Vertical active lines, lower 8 bits	40	Vertical active lines = 576 = 240 h
3C	Vertical blanking lines, lower 8 bits	31	Vertical blanking lines = 49 = 31H
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	0C	offset = 12 pixels = 0C h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	40	width = 64 pixels = 40 h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55	Vertical sync. offset = 5 lines = 05 h Vertical sync width = 5 lines
41	bits 7,6: upper 2 bits of horizontal sync. offset bits 5,4: upper 2 bits of horizontal sync pulse width bits 3,2: upper 2 bits of vertical sync offset bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	13	Horizontal image size = 531 mm = 213 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (4:3 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	00	0
46	Vertical border (pixels)	00	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table D.4 – Example detailed timing descriptor for 720x576p (50 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	D0	Horizontal active pixels = 720 = 2D0 h
39	Horizontal blanking pixels (lower 8 bits)	90	Horizontal blanking pixels = 144 = 90 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3B	Vertical active lines, lower 8 bits	40	Vertical active lines = 576 = 240 h
3C	Vertical blanking lines, lower 8 bits	31	Vertical blanking lines = 49 = 31 h
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	0C	Offset = 12 pixels = 0C h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	40	Width = 64 pixels = 40 h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55	Vertical sync. offset = 5 lines = 05 h Vertical sync width = 5 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (16:9 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	00	0
46	Vertical border (pixels)	00	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table D.5 – Example detailed timing descriptor for 720x576i (50 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	A0	Horizontal active pixels = 1440 = 5A0 h
39	Horizontal blanking pixels (lower 8 bits)	20	Horizontal blanking pixels = 288 = 120 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51	
3B	Vertical active lines, lower 8 bits	20	Vertical active lines = 288 = 120 h
3C	Vertical blanking lines, lower 8 bits	18	Vertical blanking lines = 24 = 18 h[a]
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	18	Offset = 24 pixels = 18 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7E	Width = 124 pixels = 7E h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	23	Vertical sync. offset = 2 lines[b] Vertical sync width = 3 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	13	Horizontal image size = 531 mm = 213 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (4:3 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	00	0
46	Vertical border (pixels)	00	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

[a] For interlaced display: field 1 vertical blanking = vertical blanking lines. Field 2 vertical blanking = vertical blanking lines + 1 line.

[b] For interlaced display: field 1 vertical offset = vertical sync offset. Field 2 vertical offset = vertical sync offset + 0,5 lines.

Table D.6 – Example detailed timing descriptor for 720x576i (50 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	A0	Horizontal active pixels = 1440 = 5A0 h
39	Horizontal blanking pixels (lower 8 bits)	20	Horizontal blanking pixels = 288 = 120 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51	
3B	Vertical active lines, lower 8 bits	20	Vertical active lines = 288 = 120 h
3C	Vertical blanking lines, lower 8 bits	18	Vertical blanking lines = 24 = 18 h[a]
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	18	Offset = 24 pixels = 18 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7E	Width = 126 pixels = 7E h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	23	Vertical sync. offset = 2 lines[b] Vertical sync width = 3 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (16:9 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	00	0
46	Vertical border (pixels)	00	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

[a] For interlaced display: field 1 vertical blanking = vertical blanking lines. Field 2 vertical blanking = vertical blanking lines + 1 line.

[b] For interlaced display: field 1 vertical offset = vertical sync offset. Field 2 vertical offset = vertical sync offset + 0,5 lines.

Table D.7 – Example detailed timing descriptor for 1280x720p (60 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	01	Pixel clock = 74,25 MHz
37		1D	
38	Horizontal active pixels (lower 8 bits)	00	Horizontal active pixels = 1280 = 500 h
39	Horizontal blanking pixels (lower 8 bits)	72	Horizontal blanking pixels = 370 = 172 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51	
3B	Vertical active lines, lower 8 bits	D0	Vertical active lines = 720 = 2D0 h
3C	Vertical blanking lines, lower 8 bits	1E	Vertical blanking lines = 30 = 1E h
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	6E	Offset = 110 pixels = 6E h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	28	Width = 40 pixels = 28 h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55	Vertical sync. offset = 5 lines Vertical sync width = 5 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	0	0
46	Vertical border (pixels)	0	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	1E	Flag = non-interlaced; non-stereo; digital separate; positive V sync; positive H sync

Table D.8 – Example detailed timing descriptor for 1920x1080i (60 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	01	Pixel clock = 74,25 MHz
37		1D	
38	Horizontal active pixels (lower 8 bits)	80	Horizontal active pixels = 1920 = 780 h
39	Horizontal blanking pixels (lower 8 bits)	18	Horizontal blanking pixels=280 = 118 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	71	
3B	Vertical active lines, lower 8 bits	1C	Vertical active lines = 540 = 21C h
3C	Vertical blanking lines, lower 8 bits	16	Vertical blanking lines = 22 = 16 h[a]
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	58	Offset = 88 pixels = 58 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	2C	Width = 44 pixels = 2C h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	25	Vertical sync. offset = 2 lines[b] Vertical sync width = 5 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h[c]
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	0	0
46	Vertical border (pixels)	0	0
47	Flags (bit 7 = interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	9E	Flag = interlaced; non-stereo; digital separate; positive V sync; positive H sync

[a] For interlaced display: field 1 vertical blanking = vertical blanking lines. Field 2 vertical blanking = vertical blanking lines + 1 line.

[b] For interlaced display: field 1 vertical offset = vertical sync offset. Field 2 vertical offset = vertical sync offset + 0,5 lines.

[c] Image size is display dependent. Ratio of horizontal image size to vertical image size shall be 16:9 or 4:3.

Table D.9 – Example detailed timing descriptor for 720x480p (59,94 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	D0	Horizontal active pixels = 720 = 2D0 h
39	Horizontal blanking pixels (lower 8 bits)	8A	Horizontal blanking pixels = 138 = 8A h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3B	Vertical active lines, lower 8 bits	E0	Vertical active lines = 480 = 1E0 h
3C	Vertical blanking lines, lower 8 bits	2D	Vertical blanking lines = 45 = 2D h
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	10	Offset = 16 pixels = 10 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	3E	Width = 62 pixels = 3E h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	96	Vertical sync. offset = 9 lines Vertical sync width = 6 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	13	Horizontal image size = 531 mm = 213 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (4:3 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	0	0
46	Vertical border (pixels)	0	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table D.10 – Example detailed timing descriptor for 720x480p (59,94 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	D0	Horizontal active pixels = 720 = 2D0 h
39	Horizontal blanking pixels (lower 8 bits)	8A	Horizontal blanking pixels = 138 = 8A h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20	
3B	Vertical active lines, lower 8 bits	E0	Vertical active lines = 480 = 1E0 h
3C	Vertical blanking lines, lower 8 bits	2D	Vertical blanking lines = 45 = 2D h
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	10	Offset = 16 pixels = 10 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	3E	Width = 62 pixels = 3E h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	96	Vertical sync. offset = 9 lines Vertical sync width = 6 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (16:9 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	0	0
46	Vertical border (pixels)	0	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table D.11 – Example detailed timing descriptor for 720x480i (59,94 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	A0	Horizontal active pixels = 1440 = 5A0 h
39	Horizontal blanking pixels (lower 8 bits)	14	Horizontal blanking pixels = 276 = 114 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51	
3B	Vertical active lines, lower 8 bits	F0	Vertical active lines = 240 = F0 h
3C	Vertical blanking lines, lower 8 bits	16	Vertical blanking lines = 22 = 16 h[a]
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	00	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	26	Offset = 38 pixels = 26 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7C	Width = 124 pixels = 7C h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	43	Vertical sync. offset = 4 lines[b] Vertical sync width = 3 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	13	Horizontal image size = 531 mm = 213 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (4:3 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	0	0
46	Vertical border (pixels)	0	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

[a] For interlaced display: field 1 vertical blanking = vertical blanking lines. Field 2 vertical blanking = vertical blanking lines + 1 line.

[b] For interlaced display: field 1 vertical offset = vertical sync offset. Field 2 vertical offset = vertical sync offset + 0,5 lines.

Table D.12 – Example detailed timing descriptor for 720x480i (59,94 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Notes
36	Pixel clock/10,000 (lsb stored first)	8C	Pixel clock = 27,00 MHz
37		0A	
38	Horizontal active pixels (lower 8 bits)	A0	Horizontal active pixels = 1440 = 5A0 h
39	Horizontal blanking pixels (lower 8 bits)	14	Horizontal blanking pixels = 276 = 114 h
3A	Horizontal active and blanking pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51	
3B	Vertical active lines, lower 8 bits	F0	Vertical active lines = 240 = F0 h
3C	Vertical blanking lines, lower 8 bits	16	Vertical blanking lines = 22 = 16 h[a]
3D	Vertical active: vertical blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	00	
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	26	Offset = 38 pixels = 26 h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7C	Width = 124 pixels = 7C h
40	Vertical sync offset; vertical sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	43	Vertical sync. offset = 4 lines[b] Vertical sync width = 3 lines
41	Bits 7,6: upper 2 bits of horizontal sync. offset Bits 5,4: upper 2 bits of horizontal sync pulse width Bits 3,2: upper 2 bits of vertical sync offset Bits 1,0: upper 2 bits of vertical sync pulse width	00	
42	Horizontal image size (mm, lower 8 bits)	C4	Horizontal image size = 708 mm = 2C4 h
43	Vertical image size (mm, lower 8 bits)	8E	Vertical image size = 398 mm = 18E h (16:9 in this case).
44	Horizontal and vertical image size (upper nibble = upper 4 bits of horizontal) (lower nibble = upper 4 bits of vertical)	21	
45	Horizontal border (pixels)	0	0
46	Vertical border (pixels)	0	0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

[a] For interlaced display: field 1 vertical blanking = vertical blanking lines. Field 2 vertical blanking = vertical blanking lines + 1 line.

[b] For interlaced display: field 1 vertical offset = vertical sync offset. Field 2 vertical offset = vertical sync offset + 0,5 lines.

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VESA Standards
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URL www.vesa.org

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Society of Motion Picture & Television Engineers (SMPTE), 595 West Hartsdale Avenue, White Plains, NY 10607; Phone 914-761-1100; Fax 914-761-3115
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